REMARKS

Claims 1-26 remain pending in the current Application. No Amendments to the claims have been made herein.

Rejection of claims 1-18 and 21-25 under 35 U.S.C. 102(e)

Applicants respectfully submit that claims 1-18 and 21-25 are patentable over US Patent No. 6,378,112 (hereinafter referred to as Martin) because Martin does not teach each and every element of the claims. While Martin and the current Application both address a tool for verifying two designs, the current Application recognizes and addresses problems introduced by the verification method that are not discussed or addressed in Martin. For example, the existence of false failures caused through the use of symbolic simulation (as described in the current Application) is not addressed in Martin. The current Application discusses, for example, the use of failure conditions (characterizations of a failure) and the use of additional nodes to help identify and address false failures. The additional nodes, for example, may result from the fact that an actual circuit design may include a dependency that was not apparent in the reference design. Therefore, in one embodiment of the current invention, the inputs of the two designs being verified need not match exactly. None of these issues are addressed in Martin, and since the claims of the current Application include elements which address different aspects of these previously unaddressed issues, they are not anticipated by Martin. Furthermore, under 35 U.S.C. 103(c), Martin cannot be used in a 103(a) (i.e. obviousness) rejection against the current claims because the Application and Martin are commonly assigned to Motorola, Inc.

In the Remarks section on page 8 of the current Office Action, the Examiner states that "Applicants point out that Applicants' disclosure does not recite the limitation of additional nodes. Therefore, Applicants may not rely on this point in asserting patentability of at least claim 1 in the instant Application over Martin et al." However, Applicants submit that the Examiner has misconstrued Applicants' arguments (recited above). Applicants never argued that claim 1 includes the recitation of additional nodes. In the above paragraph, Applicants were simply providing the Examiner with a better overall understanding as to how the current

Application and Martin differs, but does not address the specific claims until the following paragraphs, in which Applicants rely on the specific elements of each of claims 1, 13, 21, and 24.

For example, with respect to claims 1 and 13 and the 102(e) rejection over Martin, Applicants submit that Martin does not teach each and every element of claims 1 and 13. Claim 1 claims a tester which provides a failure indicator and a characterization of a failure in response to the detecting, the tester further comprising a failure analyzer for applying one or more constraints to the characterization of the failure, the one or more constraints representing restrictions on permissible test parameters of the second design representation, and determining whether the one or more constraints will prevent the failure from occurring. Claim 13 claims applying one or more constraints to the characterization of the failure, the one or more constraints representing restrictions on permissible test parameters of the second design representation, and analyzing the failure by determining whether the one or more constraints will prevent the failure from occurring. Martin does not teach these elements. The cited section of Martin (col. 6, lines 1-11) simply discuss the ability to test and debug a design block more quickly, but this does not teach the elements of claim 1 or claim 13 cited above, such as the use of failure indicators and characterizations of a failure or the use of constraints as claimed in claims 1 and 13. Therefore, for at least these reasons, Applicants submit that claims 1 and 13 are clearly not anticipated by Martin.

The Examiner, in the Remarks section on page 8 of the current Office Action, states that "Applicants' disclosure does not teach a failure analyzer for applying one or more constraints so in lieu of applying a 35 U.S.C. 112, first paragraph rejection to the claim, Examiner interpreted that limitation and provides cites accordingly." The Examiner proceeds to cite FIG. 2, #208, 210 and col. 6, lines 1-18 of Martin. However, Applicants submit that a failure analyzer as claimed in claim 1, in which one or more constraints representing restrictions on permissible test parameters are applied, is clearly described in the specification. For example, see FIG. 4 and corresponding text of the current Application for a full description of the application of constraints. Also, even if the Examiner broadly interprets failure analyzer, the Examiner cannot ignore the elements of claim 1 which include, for example, applying one or more constraints to the characterization of the failure, the one ore more constraints representing restrictions on permissible test parameters of the second design representation. Again, as stated above, Applicants submit that none of the cited portions of Martin teach or suggest this limitation. The

cited sections (col. 6, lines 1-16) makes absolutely no mention of applying constraints representing restriction on permissible test parameters, as claimed in claim 1. This cited section describes the advantages resulting from being able to determine that two designs are equivalent, but makes no teaching or suggestion of applying constraints to the characterization of a failure.

With respect to claims 21 and 24 and the 102(e) rejection over Martin, Applicants submit that Martin does not teach each and every element of claims 21 and 24. For example, claim 24 claims a symbolic stimulus generator that analyzes the representation of the first design to determine a set of inputs to a test point and generates a set of symbolic stimulus to be applied to corresponding test point inputs in the representation of the second design, the tester accepting as an additional input one or more additional nodes in the first design, finding additional inputs corresponding to the additional nodes, generating a second set of symbolic stimulus from the additional inputs, applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design, and generating an output response for use in verifying functional similarity. Claim 24 claims analyzing with a symbolic stimulus generator the representation of the first design to determine a set of inputs to a test point, generating a set of symbolic stimulus to be applied to corresponding test point inputs in the representation of the second design, accepting as an additional input one or more additional nodes in the first design, finding additional inputs in the first design corresponding to the additional nodes, generating a second set of symbolic stimulus from the addition inputs, and applying the second set of symbolic stimulus to corresponding inputs in the representation of the second design and generating an output response for use in verifying functional similarity. FIG. 2 and the cited sections of Martin (col. 2, line 63 to col. 3, line 67) clearly do not teach these elements. As stated above, Martin describes a symbolic assertion generator and a symbolic simulator which do not take into consideration the use of additional nodes as claimed in claims 21 and 24 which may, for example, be used to address the issue of false failures. For example, note that the inputs to symbolic assertion generation 208 of FIG. 2 in Martin include only design inputs while the inputs to symbolic assertion generation 108 of the current Application includes design inputs as well as additional reference design nodes. Therefore, for at least these reasons, Applicants submit that claims 21 and 24 are clearly not anticipated by Martin.

With respect to claims 21 and 24, the Examiner, in the Remarks section on page 8 of the current Office Action, states "Independent claims 21 and 24 recite this limitation [of additional

nodes] and it is disclosed in Martin at fig. 2, #206 which necessarily includes additional nodes, (cf. Applicants' Fig. 1, #106, the parenthetical information)." However, Applicants submit that this rejection is improper. The Examiner cannot use sections of Applicants' own specification (which are NOT indicated as being prior art) to reject the claims. That is, the reason that fig. 2, #206 of Martin did not include the additional nodes is because Martin does not teach or suggest them at all. That is, the design inputs of Martin at fig. 2, #206 ***does not necessarily include additional nodes***, as asserted by the Examiner. (See, for example, col. 2, line 60-62, of Martin which never even mentions the additional nodes while the current Application on, for example, page 6, lines 4-8, clearly includes additional nodes in the design inputs). The use of additional nodes in avoiding false failures is an aspect of the current Application (and **not** of Martin) and was thus included into FIG. 1, #106 of the current Application and also provides one of the novel aspects of claims 21 and 24. The Examiner therefore ***cannot*** use FIG. 1, #106 of the current application to conclude that this type of design input is known.

Claims 2-12, 14-18, 22-23, and 25 have not been independently addressed because they depend directly or indirectly from allowable claims 1, 13, 21, and 24, respectively, and are therefore allowable for at least those reasons stated above with respect to these claims.

Rejection of claims 19-20 and 26 under 35 U.S.C. 102(e)

Applicant respectfully submits that claims 19-20 and 26 are patentable over US Patent No. 5,754,454 (hereinafter referred to as Pixley) because Pixley does not teach or suggest each and every element of claims 19-20 and 26.

For example, with respect to claim 19, the Examiner states that the element "applying one or more constraints to the characterization of the failure ...." is taught by col. 5, lines 38-65. However, Applicants respectfully disagree. This section of Pixley teaches the screening out of invalid cutpoint pairs. Therefore is no teaching or suggestion of providing a failure indicator and a characterization of the failure, applying one or more constraints to the characterization of the failure where the one or more constraints represent restrictions on permissible test parameters of the second design representation.

In the Remarks section on page 9 of the current Office Action, the Examiner states that "Pixley's cutpoint variables represent constraints which are substituted into an XOR model to

determine a failure condition, column 6, lines 25-40," and that "Variables (constraints) are substituted and it is determined which variables result in failure." However, Applicants respectfully submit that the Examiner has mischaracterized the variables of Pixley. That is, the cutpoint variables of Pixley are not constraints *which represent restrictions on permissible test parameters*. In Pixley, when a cutpoint does not result in a match (the output of the XOR is not a one or a zero), the cutpoint is replaced with its actual function. For example, referring to FIG. 8 of Martin, the use of cutpoint variable X results in XOR_OUT being 1 for B=0 and X=1, but being 0 for the remainder of the inputs. Therefore, this cutpoint is not a valid cutpoint and is completely removed and therefore replaced with its actual function ("A or B" as seen in FIG. 5 of Pixley). Thus, cutpoint variable X is no longer present. However, cutpoint variable X is NOT a constraint which restricts permissible test parameters. That is, when cutpoint variable X is present, it can be any value *without restriction*. However, if is is invalid, it is removed all together and is therefore also not used to restrict permissible test parameters because it no longer affects the XOR circuit at all. Instead, A and B are used, where A and B can be any value, without restriction. As described in the current Application, cutpoints may be used to *generate* constraints (see, for example, page 8, line 27, through page 9, lines 8). For example, on these pages, cutpoint R216 (in FIG. 2) is introduced, where R and S are still inputs; however, cutpoint R216 is used to obtain a constraint of "R= NOT S" which restricts permissible test parameters for R and S. In Pixley, if cutpoint variable X is present, no restrictions are provided for X, and if it is removed and thus replaced by its actual function, it is no longer a test parameter. Therefore, the cutpoint variables of Pixley do not teach or suggest the constraints as claimed in claim 19. For at least these reasons, Applicants submit that claim 19 is allowable over Pixley. Claim 20, which depends from claim 19, is therefore also allowable for at least those reasons stated above with respect to claim 19.

With respect to claim 26, the Examiner states that the limitation of a symbolic stimulus generator as claimed in claim 26 is disclosed in col. 2, lines 35-57 by Pixley. Applicants respectfully disagree. This cited section of Pixley discusses binary decision diagrams (BDD), but makes no teaching or suggestion of the elements of claim 26. For example, claim 26 claims accepting as an additional input one or more additional nodes in the first design, finding additional inputs in the first design corresponding to the additional nodes, generating a second set of symbolic stimulus from the additional inputs, and applying the second set of symbolic

stimulus to corresponding inputs in the representation of the second design and generating an output response for use in verifying functional similarity, as claimed in claim 26. The cited sections of Pixley does not even teach or suggest the ability to accept additional nodes in the first design. Therefore, for at least these reasons, Applicants submit that claim 26 is not taught or suggested by Pixley.

In the Remarks section on page 9 of the current Office Action, the Examiner states that "Pixley's ATPG generates symbolic stimuli to apply to the BDD design representations" however, this is not the only element of claim 26. As discussed above, claim 26 also claims the use of additional nodes, which is not taught or suggested by Pixley.

Conclusion

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action, yet reserve the right to address them at a later time if necessary.

Applicant respectfully solicits allowance of the pending claims. Contact Joanna Chiu at (512) 996-6839 if there are any issues regarding this communication or the current Application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

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